WHAT IS CLAIMED IS:

1. A low-pass filter, comprising:

a first element block having a capacitive element;

a second element block having a resistive element, the second element block being connected in series to the first element block;

a first input terminal for receiving a first electric current, the first input terminal being provided at the side including any one of the first and second element blocks; and

a second input terminal for receiving a second electric current, the second input terminal being connected to a connection point of the first element block and the second element block,

wherein the first element block receives at least a part of the first electric current which corresponds to a difference between the electric current flowing through the second element block and the second electric current, and

the total voltage generated in the first and second element blocks is employed as an output signal.

2. The low-pass filter of claim 1, wherein:

the first input terminal is provided at the side including the second element block; and

the second electric current is an electric current whose direction is opposite to that of the first electric current and whose magnitude is N times that of the first electric current (where N is a predetermined number).

3. The low-pass filter of claim 1, wherein:

the first input terminal is provided at the side including the first element block; and

the second electric current is an electric current whose direction is the same as that of the first electric current and whose magnitude is N times that of the first electric current (where N is a predetermined number).

4. The low-pass filter of claim 1, further comprising a third element block which has a capacitive element and is provided between the first input terminal and a reference voltage.

5. The low-pass filter of claim 1, further comprising an operational amplifier which has a normal phase input terminal, an inverted phase input terminal, and an output terminal, wherein:

the first and second element blocks are provided between the inverted phase input terminal and the output terminal of the operational amplifier, and the normal phase input terminal of the operational amplifier is supplied with a reference voltage; and

the first input terminal is provided at the side including the inverted phase input terminal of the operational amplifier.

6. A low-pass filter, comprising:

a first element block having a capacitive element;

a second element block having a resistive element, the second element block being connected in series to the first element block;

an operational amplifier having a normal phase input terminal, an inverted phase input terminal, and an output terminal, the first and second element blocks being

provided between the inverted phase input terminal and the output terminal, the normal phase input terminal being supplied with a reference voltage;

a first input terminal for receiving a first electric current;

a second input terminal for receiving a second electric current, the second input terminal being connected to the inverted phase input terminal of the operational amplifier; and

a third element block having a capacitive element and a resistive element, the capacitive element being provided between the first input terminal and the reference voltage, the resistive element being provided between the first input terminal and the inverted phase input terminal of the operational amplifier,

wherein the first element block receives at least a part of the first electric current which corresponds to a difference between the electric current flowing through the resistive element of the third element block and the second electric current, and

the total voltage generated in the first and second element blocks is employed as an output signal.

7. A feedback system for feeding back an output clock generated based on an input clock such that the output clock has a predetermined characteristic, comprising:

a loop filter including a first element block which has a capacitive element, a second element block which has a resistive element and is connected in series to the first element block, a first input terminal for receiving a first electric current which is provided at the side including any one of the first and second element blocks, and a second input terminal for receiving a second electric current, which is connected to a connection point of the first and second element blocks, the first element block receiving at least a part of the first electric current which corresponds to a difference between the electric current

flowing through the second element block and the second electric current, the total voltage generated in the first and second element blocks being employed as an output signal;

a charge pump circuit for generating the first and second electric currents based on a phase difference between the input clock and the fed-back clock; and

output clock generation means for generating the output clock based on the output signal from the loop filter.

8. The feedback system of claim 7, wherein the output clock generation means is a voltage controlled oscillator which oscillates the output clock and changes the oscillation frequency based on the output signal from the loop filter.

9. The feedback system of claim 7, wherein the output clock generation means is a voltage controlled delay circuit which changes a delay amount of the output clock with respect to the input clock based on the input clock and the output signal from the loop filter.

10. The feedback system of claim 7, wherein:

the first input terminal of the loop filter is provided at the side including the second element block;

the direction of the second electric current is opposite to that of the first electric current, and the magnitude of the second electric current is N times that of the first electric current (where N is a predetermined number); and

the charge pump circuit includes a first partial charge pump circuit which outputs/receives the first electric current and a second partial charge pump circuit which outputs/receives the second electric current.

11. The feedback system of claim 7, wherein:

the first input terminal of the loop filter is provided at the side including the second element block;

the direction of the second electric current is opposite to that of the first electric current, and the magnitude of the second electric current is N times that of the first electric current (where N is a predetermined number); and

the charge pump circuit includes a first partial charge pump circuit which outputs/receives an electric current corresponding to a difference between the first electric current and the second electric current and a second partial charge pump circuit which outputs/receives the second electric current, the charge pump circuit combining the electric currents output from/received by the first and second partial charge pump circuits to obtain the first electric current.

12. The feedback system of claim 7, wherein:

the first input terminal of the loop filter is provided at the side including the first element block;

the direction of the second electric current is the same as that of the first electric current, and the magnitude of the second electric current is N times that of the first electric current (where N is a predetermined number); and

the charge pump circuit includes a first partial charge pump circuit which outputs/receives the first electric current and a second partial charge pump circuit which outputs/receives the second electric current.

13. A semiconductor integrated circuit comprising the low-pass filter of claim 1.

14. A semiconductor integrated circuit comprising the feedback system of claim 7.

15. The semiconductor integrated circuit of claim 14, wherein the semiconductor integrated circuit is used in an IC card.

16. The semiconductor integrated circuit of claim 14, wherein:

the semiconductor integrated circuit has a chip-on-chip structure; and

the feedback system is incorporated in an upper layer of the chip-on-chip structure.

17. The semiconductor integrated circuit of claim 14, wherein the feedback system is incorporated in a pad region of the semiconductor integrated circuit.

18. The semiconductor integrated circuit of claim 14, wherein the semiconductor integrated circuit is a microprocessor.